AMENDMENTS TO THE CLAIMS:

1. (Currently Amended) A differential amplifier circuit comprising a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit;

a fourth transistor for supplying a the drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; and

said third transistor is connected in parallel to said fourth transistor.

2. (Canceled)

3. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of said differential amplifier circuit.

4. (Canceled)

5. (Currently Amended) The differential amplifier circuit as claimed in claim 1, wherein the control electrode of said third transistor is supplied with a first control signal for ~~constantly~~ supplying the minute current during the operation of said differential amplifier and a second control signal for supplying the drive current.

6. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein a gate width of said third transistor is smaller than a gate width of said fourth transistor.

7. (Canceled)

8. (Previously Presented) The differential amplifier circuit as claimed in claim 1, wherein a first control signal supplied to the control electrode of said third transistor is set to a level for supplying a predetermined current as the drive current at the time of signal determination in said differential amplifier circuit, while causing the minute current to flow through said first and second transistors at other than the time of signal determination during the operation of said differential amplifier.

9. (Original) The differential amplifier circuit as claimed in claim 1, wherein said latch unit comprises:

a first inverter inserted between the second electrode of said first transistor and a second power line; and

a second inverter inserted between the second electrode of said second transistor and said second power line, said first and second inverters being cross-coupled to each other.

10. (Original) The differential amplifier circuit as claimed in claim 9, wherein:

said differential amplifier circuit is configured of MOS transistors;

transistors of said first and second inverters which are connected to said second power line are each connected in parallel to an additional transistor, respectively; and

the second electrode of each of said first and second transistors is held at a predetermined level at other than the time of signal determination during the operation of said differential amplifier.

11. (Previously Presented) The differential amplifier circuit as claimed in claim 1, further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor for shorting the second electrodes of said first and second transistors in accordance with a second control signal.

12. (Original) The differential amplifier circuit as claimed in claim 1, further comprising:

a sixth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor, said sixth transistor having a control electrode supplied with a predetermined voltage.

13. (Original) The differential amplifier circuit as claimed in claim 12, wherein said differential input signal is at CML level.

14. (Original) The differential amplifier circuit as claimed in claim 1, further comprising:

a seventh transistor inserted between two nodes for retrieving a differential output signal, said seventh transistor shorting said two nodes in accordance with a third control signal.

15. (Previously Presented) The differential amplifier circuit as claimed in claim 1, further comprising:

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

16. (Original) The differential amplifier circuit as claimed in claim 1, wherein said differential amplifier circuit is a differential sense amplifier circuit of strong arm latch type.

17. (Currently Amended) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with the ~~a~~ differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit;

a fourth transistor for supplying the ~~a~~ drive current at the time of signal determination in said differential amplifier circuit is inserted between said first power line and the common node to which the first electrodes of said first and second transistors are connected; and

said third transistor is connected in parallel to said fourth transistor.

18. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said semiconductor integrated circuit is a receiving circuit of a signal transmission system, said signal transmission system comprising a transmission circuit outputting the differential signal, a signal transmission path, and said receiving circuit receiving the differential signal through said signal transmission path.

19. (Currently Amended) The semiconductor integrated circuit device as claimed in claim 18, wherein the receiving circuit further ~~comprising~~ comprises:

an equalizer circuit~~, receiving~~ coupled between the transmission circuit and the amplifier circuit, wherein the equalizer circuit receives the differential signal, removing an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and outputting the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

20. (Currently Amended) A ~~semiconductor integrated~~ circuit device comprising:

a transmission circuit outputting a differential signal;

a signal transmission path; and

a receiving circuit receiving the differential signal through said signal transmission path, wherein

the receiving circuit comprises a plurality of receiving units, said plurality of receiving units carrying out an interleave operation, and wherein

each of the plurality of receiving units ~~comprise~~ comprises:

~~a semiconductor integrated circuit device having~~ a differential amplifier circuit receiving [[a]] an Inter-Symbol Interference removed differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with the Inter-Symbol Interference removed ~~a~~ differential input signal; ~~and~~

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, wherein said third transistor also supplies a drive current at the time of signal determination in said differential amplifier circuit; and

~~wherein said semiconductor integrated circuit is a receiving circuit of a signal transmission system, said signal transmission system comprising a transmission circuit outputting the differential signal, a signal transmission path, and said receiving circuit receiving the differential signal through said signal transmission path.~~

an equalizer circuit, receiving the differential signal, removing an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and outputting the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

21. (Canceled)

22. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein said third transistor turns off said minute current flowing through said first and second transistors upon deactivation of said differential amplifier circuit.

23. (Canceled)

24. (Currently Amended) The semiconductor integrated circuit device as claimed in claim ~~23~~ 17, wherein the control electrode of said third transistor is supplied with a first control signal for ~~constantly~~ supplying ~~a~~ the minute current during the operation of said differential amplifier and a second control signal for supplying the drive current.

25. (Currently Amended) The semiconductor integrated circuit device as claimed in claim ~~23~~ 17, wherein a gate width of said third transistor is smaller than a gate width of said fourth transistor.

26. (Canceled)

27. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein a first control signal supplied to the control electrode of said third transistor is set to a level for supplying a predetermined current as the drive current at the time of signal determination in said differential amplifier circuit, while causing the minute current to flow through said first and second transistors at other than the time of signal determination during the operation of said differential amplifier.

28. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said latch unit comprises:

a first inverter inserted between the second electrode of said first transistor and a second power line; and

a second inverter inserted between the second electrode of said second transistor and said second power line, said first and second inverters being cross-coupled to each other.

29. (Original) The semiconductor integrated circuit device as claimed in claim 28, wherein:

said differential amplifier circuit is configured of MOS transistors;

transistors of said first and second inverters which are connected to said second power line are each connected in parallel to an additional transistor, respectively; and

the second electrode of each of said first and second transistors is held at a predetermined level at other than the time of signal determination during the operation of said differential amplifier.

30. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a fifth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor for shorting the second electrodes of said first and second transistors in accordance with a second control signal.

31. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a sixth transistor connected to the second electrode of said first transistor and the second electrode of said second transistor, said sixth transistor having a control electrode supplied with a predetermined voltage.

32. (Original) The semiconductor integrated circuit device as claimed in claim 31, wherein said differential input signal is at CML level.

33. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

a seventh transistor inserted between two nodes for retrieving a differential output signal, said seventh transistor shorting said two nodes in accordance with a third control signal.

34. (Previously Presented) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit further comprising:

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal.

35. (Original) The semiconductor integrated circuit device as claimed in claim 17, wherein said differential amplifier circuit is a differential sense amplifier circuit of strong arm latch type.

36. (Currently Amended) A receiving circuit of a signal transmission system, said signal transmission system comprising a transmission circuit outputting a differential signal, a signal transmission path, and said receiving circuit receiving the differential signal through said signal transmission path, the receiving circuit comprising a receiving unit, wherein the receiving unit comprises:

a differential amplifier circuit, said differential amplifier circuit including a latch unit and a differential input portion, wherein a minute current is kept to flow through said differential input portion;

a latch circuit latching an output signal of said differential amplifier circuit;

a clock source generating a clock and supplying the generated clock to said differential amplifier circuit; and

an equalizer circuit~~,~~ for receiving the differential signal, removing an Inter-Symbol Interference of the differential signal by a Partial Response Detection, and outputting the Inter-Symbol Interference removed differential signal to said differential amplifier circuit.

37. (Currently Amended) The receiving circuit of a signal transmission system as claimed in claim 36, wherein the receiving circuit ~~comprises a plurality of~~ further comprises at least one additional receiving ~~units~~ unit, each additional receiving unit including said differential amplifier circuit, said latch circuit and said equalizer circuit, said ~~plurality of~~ receiving ~~units~~ circuit carrying out an interleave operation.

38. (Previously Presented) A differential amplifier circuit comprising a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with a differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, a gate electrode of said third transistor receiving a control signal of which level is changed in accordance with the operation of said differential amplifier circuit; and

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are connected, the control electrode of said eighth transistor being supplied with a fourth control signal, wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier circuit.

39. (Currently Amended) A semiconductor integrated circuit device having a differential amplifier circuit receiving a differential signal, a latch circuit latching an output signal of said differential amplifier circuit, and a clock source generating a clock and supplying the generated clock to said differential amplifier circuit, wherein said differential amplifier circuit comprises a latch unit and a differential input portion, wherein:

said differential input portion comprises a first transistor and a second transistor each having a first electrode, a second electrode and a control electrode;

the control electrodes of said first and second transistors are supplied with the ~~a~~ differential input signal;

a third transistor for keeping a minute current to flow through said first and second transistors is inserted between a first power line and a common node to which the first electrodes of said first and second transistors are connected, a gate electrode of said third transistor receiving a control signal of which level is changed in accordance with the operation of said differential amplifier circuit; and

an eighth transistor inserted between a second power line and the common node to which the first electrodes of said first and second transistors are

connected, the control electrode of said eighth transistor being supplied with a fourth control signal, wherein the third transistor doubles as a transistor for supplying a drive current at the time of signal determination by said differential amplifier current.